ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

PERFORMANCE ANALYSIS OF MULTICARRIER SPWM STRATEGIES FOR THREE PHASE Z-SOURCE SEVEN LEVEL CASCADE INVERTER

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ABSTRACT

Multilevel inverter is one of the attractive topology for DC to ac conversion. Multilevel inverter synthesizes desired voltage wave shape from several levels of DC voltages. But main drawback of MLI is its output voltage amplitude is limited to the DC sources voltage summation.

To overcome this limitation a five level Z source cascaded H bridge multilevel inverter has been proposed here. In the proposed topology output voltage amplitude is boosted with the Z network shoot through state control. It employs the Z network between DC source and inverter circuitry to achieve the boost operation. Output voltage of proposed inverter is controlled using modulation index and shoots through state. The Performance parameters of Z Source Multilevel inverter is analyzed for unipolar modulation and space vector modulation.

In this thesis multilevel inverter based Z source is proposed which can solve above mentioned problems. The Z source inverter utilizes Z impedance network between the DC source and the inverter circuit to achieve buck boost operation. It utilizes shoot through state control to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The Z Source inverters have advantages such as lower costs reliable lower complexity and higher efficiency. Simulation model of Z source cascaded multilevel inverter with unipolar ISCPWM unipolar CDPWM and SVM Modulation technique has been built in MATLAB/SIMULINK and its performance has been analyzed.

KEYWORDS: Multi Level Inverter, Total Harmonic Distortion, Pulse Width Modulation, Shoot-Through, Buck-Boost.

INTRODUCTION

Multilevel inverters are widely used in high power applications such as large induction motor drives UPS systems and Flexible AC Transmission Systems (FACTS). Multilevel inverter obtains the desired output voltage from several levels of input DC voltage sources. Increasing the number of DC voltage sources the inverter output voltage level will be increased. The multilevel inverters has advantages such as lower semiconductor voltage stress better harmonic performance low Electro Magnetic Interference and lower switching losses. These advantages multilevel inverters output voltage amplitude is limited to the input DC sources voltages summation. It requires an intermediate DC to DC converter is for the buck or boost converter operation of MLI output voltage. Also occurring of short circuit will destroy multilevel inverters. In this paper multilevel inverter based Z source is proposed which can solve above mentioned problems. The Z source inverter used Z impedance network between the DC source and the inverter circuit to achieve buck boost operation. It utilizes shoot through state control to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The Z Source inverters have advantages such as lower costs reliable lower complexity and higher efficiency.

The AC output voltage can be of fixed or variable frequency and it can be achieved either by controlled turn on and turn off devices (e.g. BJTs MOSFETs IGBTs and GTOs) or by forced commutated thyristors depending on applications. Ideal inverter output voltage waveforms will be sinusoidal. The practical inverters voltage waveforms are non sinusoidal and contain some certain harmonics. The output frequency of an inverter is finding by the rate at which the semiconductor devices are switched on and off by the control circuit and can provide ac output of adjustable

frequency. The dc input to the inverter may be a battery fuel cell solar cell or other dc sources. But in case industrial applications and it is fed by a rectifier.

Motivation and Objectives

In this thesis a single phase cascaded H bridge five levels Z Source inverter is proposed for renewable energy systems and it employs Z network between the DC source and inverter circuitry to achieve boost operation. The output voltage inverter can be controlled using modulation index and shoot through state control. Cascaded Z Source Multilevel inverter is analyzed with unipolar inverse sine carrier unipolar carrier disposition PWM SVM techniques. Performance parameters have been analyzed for cascaded Z Source multilevel inverter. The performances of the three techniques are compared for single phase 5 levels Z Source cascaded multilevel inverter. Simulations of the circuit configurations have been performed.

To overcome the problems of the traditional Voltage and current source converters presents an impedance source (impedance fed) power converter (Z source converter) and its control method for implementing dc to ac power conversion. It employs a unique impedance network to couple the inverter main circuit to the power source for providing unique features that cannot be observed in the traditional Voltage and current source converters where a capacitor and inductor are used. The Z source converter overcomes the above mentioned limitations of the traditional Voltage and current source converter and provides a novel power conversion concept. In Fig. a two port network that consists of a split inductor L1 and L2 and capacitors C1 and C2connected in X shape is employed to provide an impedance source (Z source) coupling the converter (or inverter) to the dc source. The dc source or load is a voltage or a current source or load. Therefore the dc source is a battery diode rectifier thyristor converter fuel cell and inductor a capacitor or a combination of those. A switch used in the converter is a combination of switching devices and diodes such as the anti parallel combination the series combination etc.

TOPOLOGIES OF MULTILEVELCONVERTERS

Diode Clamped Multilevel Inverter

Today's the most commonly used multilevel topology is the diode clamped inverter and the diode is works as the clamping device to clamp the dc bus voltage to achieve steps in the output voltage. In Figure 3.1 show the circuit for a diode clamped inverter for a three level and a four level inverter. The difference between two level inverter and three level inverter are the diodes D1a and D2a and these two devices clamp the switch voltage to half the level of the DC bus voltage. The voltage across every capacitor for an N level diode clamped inverter at steady state is Vdc / n −1.

Each active switching device is only required to block Vdc / n −1 the clamping devices has different ratings. The diode clamped inverter gives multiple voltage levels by connecting of the phases to a series of capacitors. By the aboriginal invention the concept is extended to any number of levels by increasing the number of capacitors in the circuit. An early description of this topology is limited to three levels and where two capacitors are connected across the dc bus resulting in one extra level. The extra level is neutral point of the DC bus so that the terminology neutral point clamped inverter is introduced here. With an even number of voltage levels neutral point is not available and the term multiple points clamped is sometimes applied in the circuit. Due to capacitor voltage balancing problem the diode clamped inverter implementations have been limited to the three levels inverter. Because of industrial developments in the past years the three level inverter is today's used extensively in industry applications. The most applications are medium voltage a three level inverter for 480V.

In general for an N level diode clamped inverter for each leg 2 (N-1) switching devices (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N which is neutral point is sufficiently high the number of diodes and the number of switching devices is increase and make the system difficult to implement.

If the inverter runs under the Pulse Width Modulation diode reverse recovery of these clamping diodes create the major problem which is challengeable.

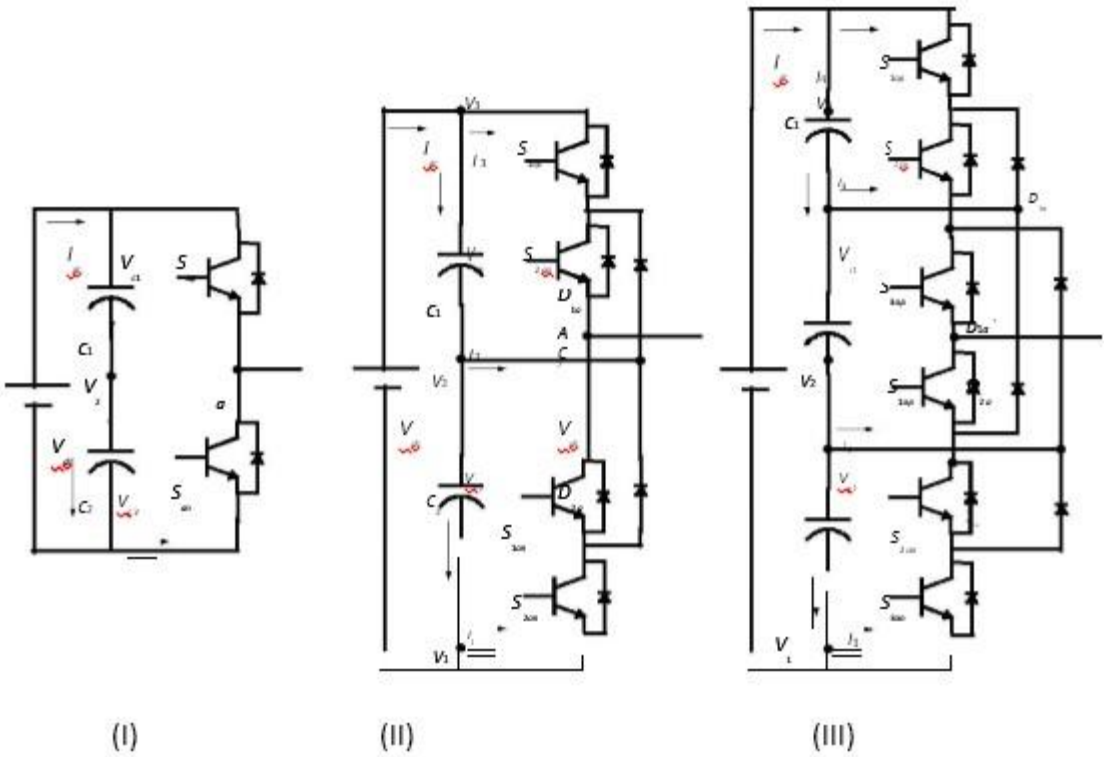


Figure 2.1: (I) two level inverter (II) three level inverter (III) four level inverter

Though the structure is more complicated than the two inverter the operation is straight forward. In summary each phase node (*a b* or *c*) can be connected to any node in the capacitor bank (V_3 V_2 V_1*)*. Connection of the a phase to positive node V_3 occurs when S_{1ap} and S_{2ap} are turned on and to the neutral point voltage when S_{2ap} and S_{1an} are turned on and the negative node V_1 is connected when S_{1an} and S_{2an} are turned on. There are some complementary switches are used and in the practical improvement some dead time is included between the signals .Their complements meaning that both switches in a complementary pair is switched off for a small amount of time during a transition.

For the practical discussion here in the dead time is ignored. From Figure 2.1 (II) shown that with this switching state the ***a*** phase current I_a will flow into the junction through diode D_{1a} and if the current is negative or out of the junction through diode D_{2a} the current is positive. The DC currents I_3 currents I_2 and I_1 currents are the node currents of the inverter. Increasing the diode clamped to four levels results in the topology described in Figure 3.1 (III). Two diodes are added in each phase for the two junctions. The operation is similar to the three levels. For practical improvement the switching state needs to be converted into transistor signals. Once the transistor signals are connected in expressions for the *a* phase line to ground voltage and the *a* phase component of the DC currents written as

$$V_{ao} = H_{aN} V_{N0} + H_{aN-1} V_{N-10} + \ldots + H_{a1} V_{10} \quad (2.1)$$

$$V_{bo} = H_{bN} V_{N0} + H_{bN-1} V_{N-10} + \ldots + H_{b1} V_{10} \quad (2.2)$$

$$V_{co} = H_{cN} V_{N0} + H_{cN-1} V_{N-10} + \ldots + H_{c1} V_{10} . \quad (2.3)$$

The node currents for the N level inverter given by

$$I_N = H_{aN} I_a + H_{bN} I_b + H_{cN} I_c$$

$$I_{N-1} = H_{aN-1} I_a + H_{bN-1} I_b + H_{cN-1} I_c$$

$$I_1 = H_{a1} I_a + H_{b1} I_b + H_{c1} I_c .$$

The above relationships can be programmed into simulation software to form a block that simulates one phase of a diode clamped inverter. The number of blocks is connected together for a multiphase system. For more details the transistor and diode KVL and KCL equations will be implemented. This allows insertion of device voltage drops as well as conduction losses and also the individual device voltages and currents. To explain these relationships consider the general N level diode clamped structure. Therein only the upper half of the inverter is considered since the lower half contains complementary transistors and analyzed in a similar way. The clamping action of diodes the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank.

The inner diodes of the multilevel inverter are blocking a higher voltage and for example in the four level topology the inner diodes block two thirds of the dc voltage while the outer diodes block one third. This is a disadvantage of the diode clamped topology. Thus this reason some authors represent the higher voltage diodes with lower voltage diodes in series or change the structure of the topology so that each diode blocks the same voltage.

Cascaded Multilevel Inverter

Cascaded multilevel inverters are series connected full bridge inverters each with their own isolated dc bus. This multilevel inverter can generate sinusoidal waveform voltage from several separate dc sources. This type of converter does not need any types of transformer clamping diodes or flying capacitors. Every level generates three different voltage outputs +Vdc zero and –Vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of multilevel inverter is the sum of all the individual inverter outputs. Each of the H Bridges active devices switches only at the fundamental frequency and these frequencies generates a quasi square waveform by phase shifting its positive and -Ve phase shift legs switching timings. Furthermore each switching device always conducts for 180˚ or half cycle regardless of the pulse width of the quasi square wave. This switching method results in equalizing the current increase in active device.

This topology of inverter is suitable for high voltage and high power reversal because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. For the simplification of the circuit and advantages Cascaded H bridge topology is selecting for the presented thesis. The multilevel inverter has four main advantages firstly the voltage stress in every switch is decreased due to series connection of the switches therefore the rated voltage and consequently the total power of the inverter will be safely increased. And secondary the rate of change of voltage dV/dt is decreased due to the lower voltage swing of switching cycle. Third harmonic distortion is reduced in this switching cycle. Fourth lower acoustic noise and electromagnetic interference EMI is obtained in the device.

Mixed Level Hybrid Multilevel Cells

The hybrid converter topology is proposed by Mr.Manjrekar. Gating the high voltage high power applications it is possible to adopt multilevel diode clamped or capacitor clamped inverters to replace the full bridge cell in a cascade inverter. The reason for this replacement is to reduce the amount of separate dc sources. The cascade inverter requires more number of dc sources than the mixed hybrid inverter to achieve the same number of levels.

Figure 3. Shows the structure of a seven level hybrid inverter in which seen that each phase leg is constructed from a high voltage stage and a low voltage stage. The simplest configuration includes two series connected dingle phase inverters per phase with their dc voltages in the ration of 2:1. In the operation the hybrid converter uses the High Voltage stage to achieve the bulk power transfer and uses the low voltage stage that means to improve the spectral performance of the overall converter. The levels gating using the configuration in Figure 3. Are $3V_{dc}$ $2V_{dc}$ V_{dc} 0 $-V_{dc}$ $-2V_{dc}$ - $3V_{dc}$. Also note that the High Voltage stage is shown to be constructed using devices that have high voltage blocking characteristics but not necessarily fast switching characteristics like integrated gate controlled thyristors IGCT while the Low Voltage stage is constructed using devices that have fast switching characteristics but not necessarily high voltage blocking characteristics like insulated gate bipolar transistor .

The hybrid system again uses the transformer to produce the isolated dc supplies for each full bridge inverter and the

control of the converter is more complex than the standard cascaded connection. However the control is still modular in that the Low Voltage stage and High Voltage stage have their own reference waveforms but the Low Voltage stage reference must be created from the High Voltage reference. One of the problems with the converter is that during the middle ranges of the modulation index the High Voltage stage will be supplying more power to the load when compared to the Low Voltage stage. Under these operating conditions the Low Voltage stage required to operate in a rectification mode that means that the DC link must be Capable in both directional.

CONTROL SCHEMES

The main aim of the modulation methods in multilevel inverters is to synthesize the output voltage as possible to the sinusoidal waveform. Many modulation methods have been developed for harmonic reduction and switching loss minimization. Multilevel inverter control methods are based on fundamental and high switching frequency. Another commonly used classification for the modulation methods developed to control the multilevel inverters which is depend upon open loop and closed loop abstraction.

UNIPOLAR MCPWM TECHNIQUE

Unipolar MCPWM technique is obtained by comparing the rectified sinusoidal reference or with two sine references sine and 180 degree phase shifted sine wave with multi carriers positioned above the zero level. These techniques have the advantage of effectively doubling the switching frequency as far as the output harmonics frequency are concerned where the lowest harmonics frequency appears as side bands of twice switching frequency and Here n numbers of carriers are required for calculating 2n+1 level in above methods.

UNIPOLAR ISCPWM

The control methods uses an inverted high frequency sine carrier that helps to increasing the output voltage for a given modulation index. For maximize fundamental component demands greater pulse area. The difference in pulse widths of signals and get resulting from triangle wave and inverted sine wave with the low output frequency reference sine wave is easily understood.

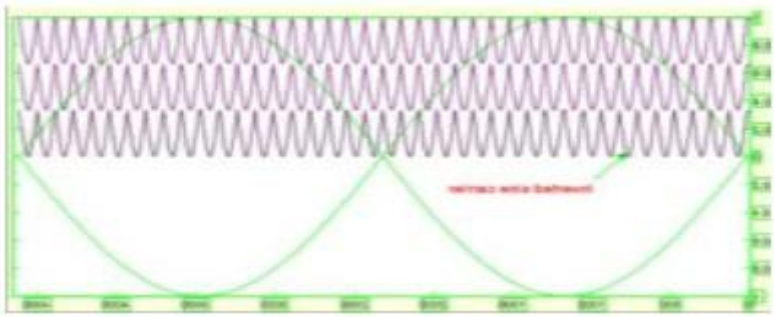


Fig.3.1 Unipolar Iscpwm

UNIPOLAR CDPWM

In this method four phase shifted carrier triangular signals are compared with the two modulating sinusoidal signals to produce switching Pulse Width Modulation pulses. These methods involve two straight lines and these lines are greater than or less than the peak value of the reference sinusoidal signal to control through the duty ratio. The Inverter operates in shoot through whenever the triangular carrier signal is higher than positive straight line or lower than the negative straight line. The frequency of modulating signal is taken as 50Hz. The frequency of the triangular signal is intended by Frequency modulation index mf and which is given.

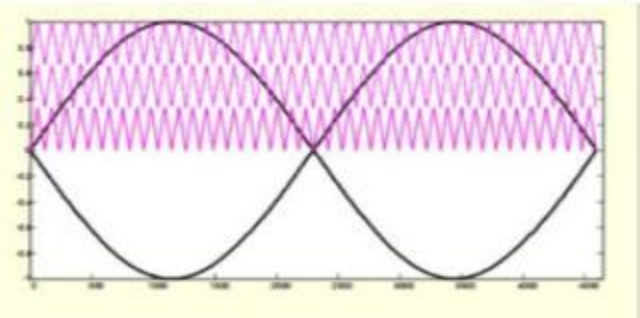


Fig.3.2 Unipolar Cdpwm

For full bridge inverters the output voltages are given by where fc is the frequency of the carrier signal and f_o is the sinusoidal frequency and modulating signals. Output voltage which is depends on the boost factor.

$B=1/ \{1-[2(V_{ca}-V_p)]/V_{ca}\}$

$=1/ (1-2T_{sh}/T)$ (5)

V_{ca}: maximum value of the triangular waveform

V_p: Amplitude of the constant

T_{sh}: Total shoot through state period

SPACE VECTOR MODULATION

The SVM technique can be easily extended to all types of multi level inverters. In Fig. 5 describes space vectors for the traditional used two level three level and five level inverters. These vector diagrams are universal despite of the type of multilevel inverter. And Fig.5 it is valid for five level diode clamped capacitor clamped or cascaded inverter. The adjacent three vectors is synthesize a desired voltage vector by computing the duty cycle Tj Tj+1and Tj+2 for each vector V=((TjVj+Tj+1Vj+1+Tj+2Vj+2))/T (6)

Space vector Pulse Width Modulation methods generally have the following features like as good utilization of dc link voltage low current ripple and relatively easy hardware implementation by a digital signal processor . These implemented techniques make it suitable for high voltage high power applications. If the number of levels increases unessential switching and the complexity of selecting switching states increase radicalmente. Some user have used decomposition of the five level space vector diagram into two three level space vector diagrams with a phase shift to minimize ripples and simplify control. Additionally a simple space vector selection method is introduced without duty cycle computation of the adjacent three vectors.

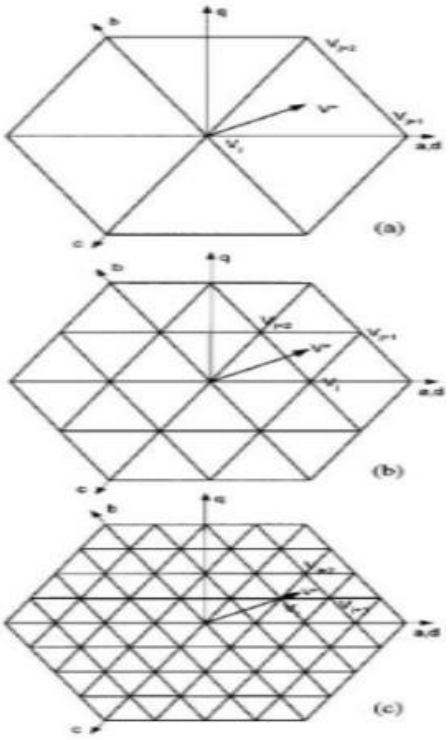


Fig.3.3 Space vector diagram: (a) two level (b) three level and (c) five level inverter.

Modelling Of Cascaded H Bridge Inverter

For every full bridge inverter the output voltage:

$V_{oi}=V_{di}(S_1i-S_2i)$ (1)

Input dc current :

$I_{dci}=I_a(S_1i-S_2i)$ (2)

Where

i =1 2... Number of full bridge inverters employed.

Ia = output current of the cascaded inverter.

S_1i and S_2i = the upper switch of each full bridge inverter.

Output voltage of the phase of the multilevel cascaded inverter is:

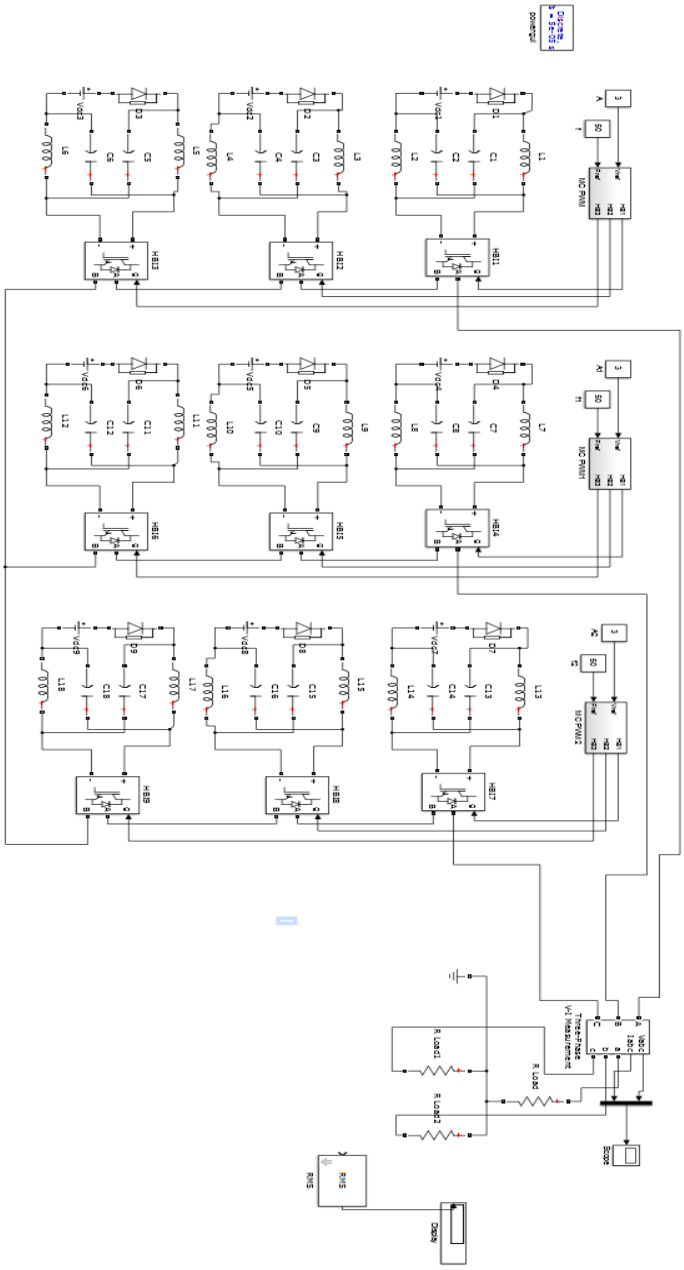
$V_{on}=\sum V_{oi}$ i = 1 2....n (3)

Matlab Model of Seven Level Inverter

The Z-source cascaded seven level inverter is modeled in SIMULINK using power system block set. Switching signals for cascaded multilevel inverter using MCSPWM strategies are simulated. Simulations are performed for different values of m_a ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are listed in Table I. Figure 8-17 show Simulations are performed for different values of m_a ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are listed in Table I. the Switching

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

signals for cascaded multilevel inverter using MCSPWM strategies are simulated. simulated output voltage of Z source CMLI and their harmonic spectra. Figure 8 displays the seven level output voltage generated by PDPWM switching strategy and its FFT plot is shown in Figure 9. Figure 10 shows the seven level output voltage generated by PODPWM strategy and its FFT plot is shown in Figure 11. Figure 12 shows the seven level output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 13. Figure 14 shows the seven level output voltage generated by COPWM strategy and its FFT plot is shown in Figure 15. Figure 16 shows the seven level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure 17. Tables II and III displayed the V_{RMS} (fundamental) of the output voltage and Crest Factor (CF) for various modulation indices of Z -Source seven level cascaded inverter respectively.



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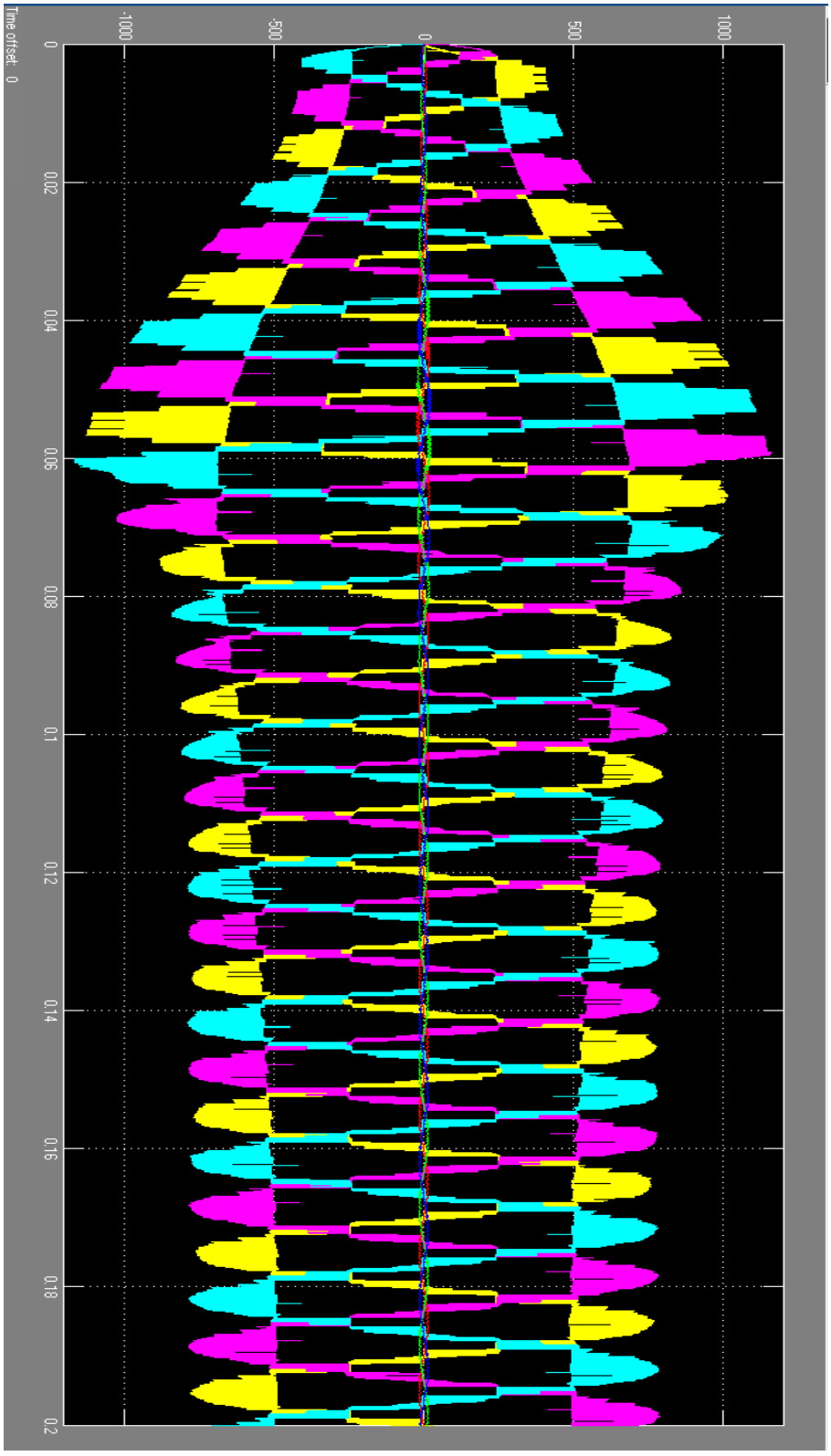
Simulation Results



The following parameter values are used for simulation: V_1 =50V, V2=50V, V_3=50V, R (load) = 100 ohms, f_c=1000 Hz and f_m=50Hz.

CONCLUSION

In this thesis MCSPWM strategy for three phase Z source seven level cascaded inverter have been presented. The Z source cascaded seven level inverter is modeled in SIMULINK using power system block set. The Switching signals for cascaded multilevel inverter using MCSPWM strategies are simulated. The Simulations are performed for different values of m_a ranging from 0.8 to 1 and corresponding percentage THD measured using the FFT block and their values are listed. The simulated output voltage of Z source CMLI and their harmonic spectra and Z source multilevel inverter gives higher output voltage through its Z source network. The Performance factors like percentage THD VRMS and CF have measured and analyzed. found that the PODPWM strategy provides lower percentage THD and higher VRMS and less number of dominant harmonics than the other strategies. The DC source is replaced by renewable energy sources and this Z source seven level cascaded inverter can be used for distributed generation systems.

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